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(54) Thin film negative temperature coefficient resistor structures

(57) Thin film negative temperature coefficient (NTC) thermistors (10,11,12,13,14,15) can be fabricated with mutual thermal coupling whilst remaining electrically isolated to form slow speed logic devices. If both thermistors 10 and 11 are driven to the negative resistance state by applied voltages they will heat thermistor 12. This structure functions as an AND gate. If either thermistor 13 or thermistor 14 is driven to the negative resistance state thermistor 15 will be heated. This structure functions as an OR gate. Switching speeds are fast enough for e.g. protective circuits for electrical equipment.

Fig.5.

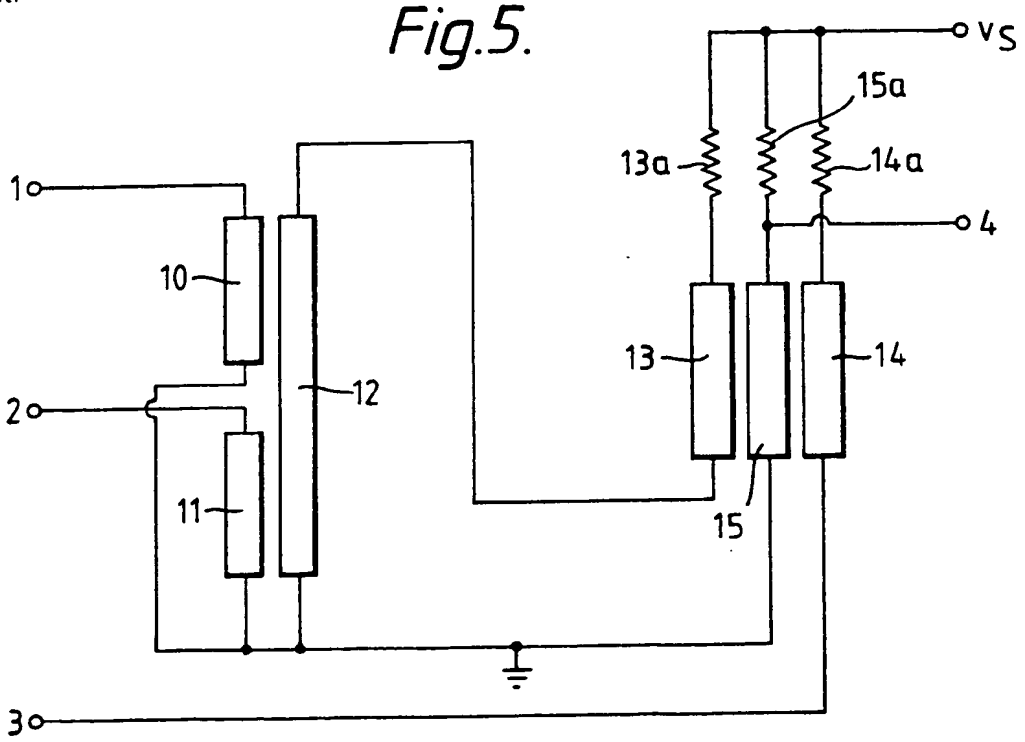

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Fig.1.

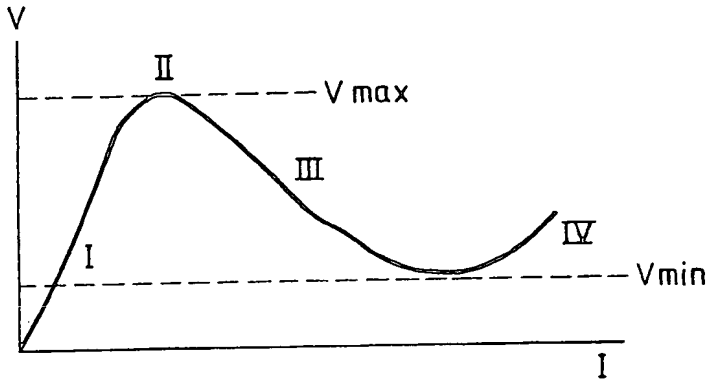
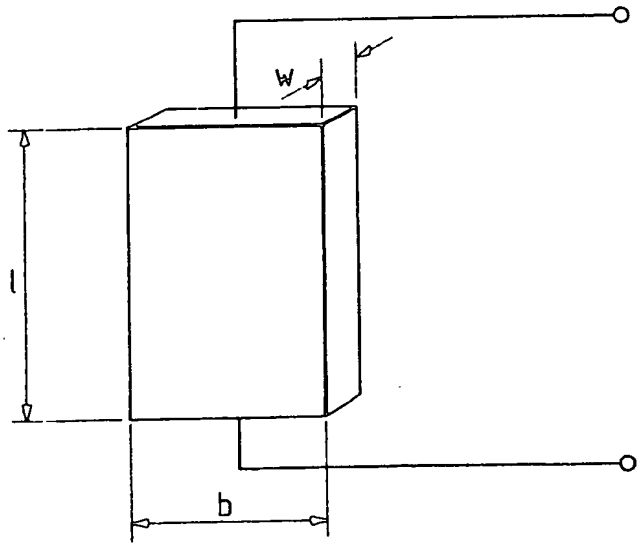


Fig.2.



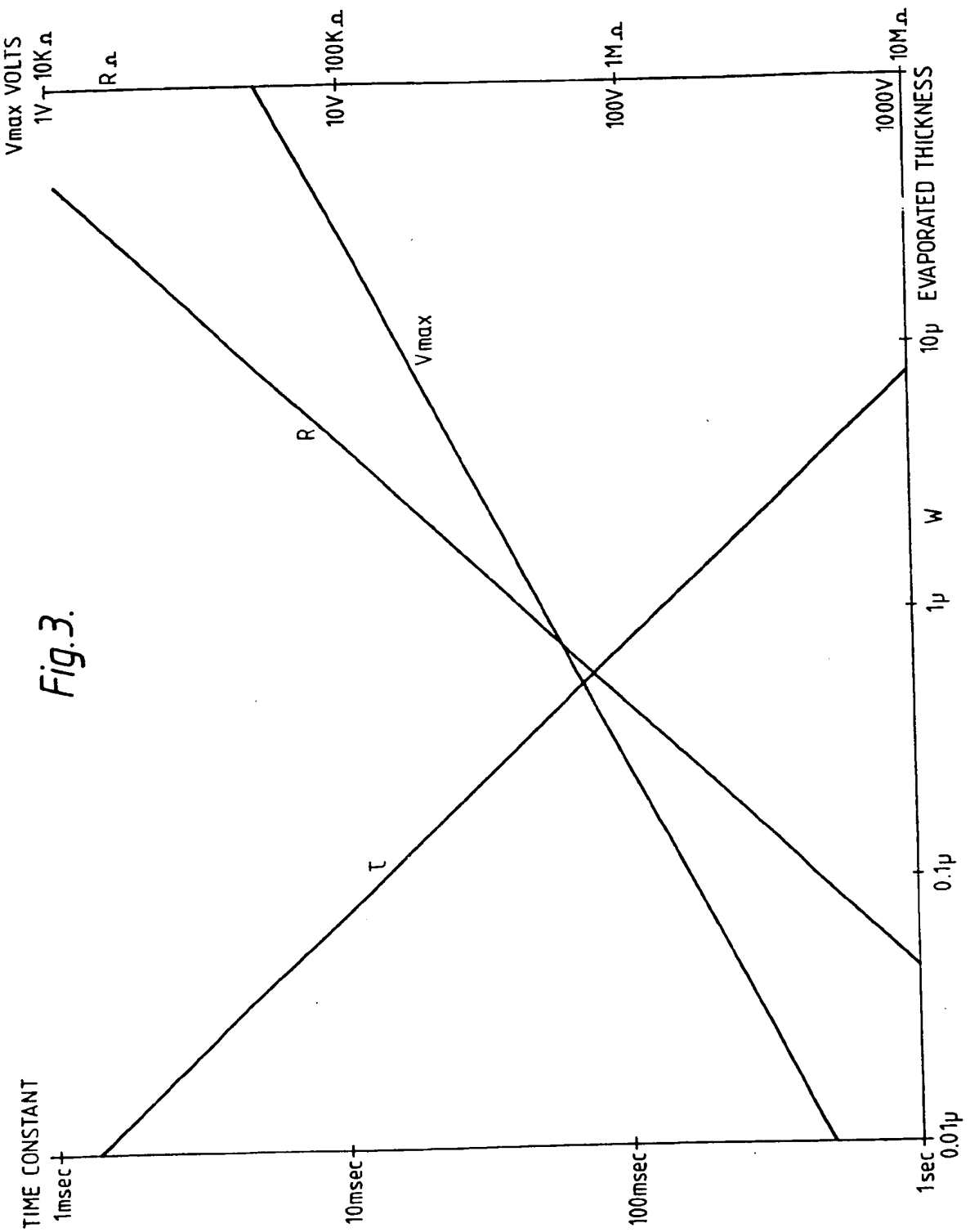


Fig.3.

Fig.4.

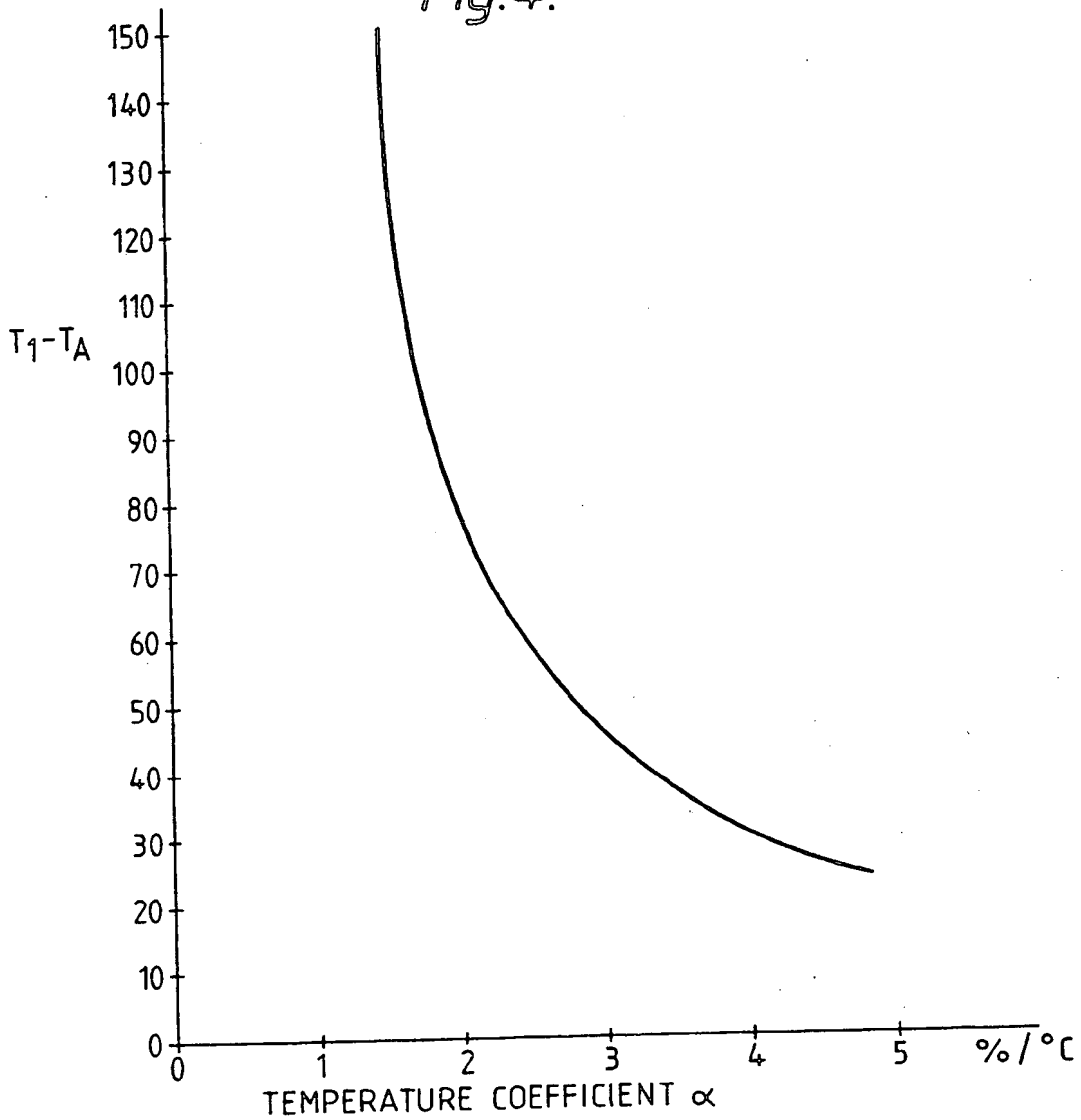
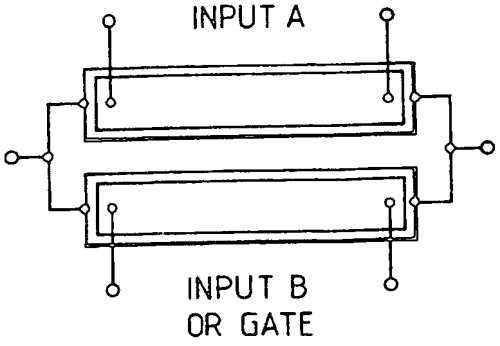


Fig.7.



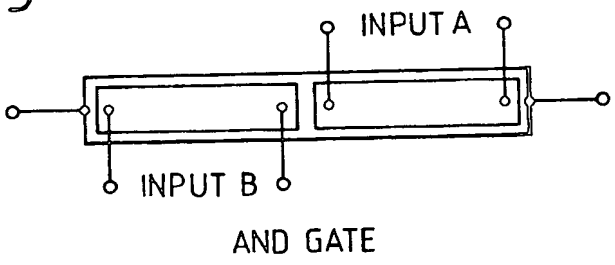


Fig.5.

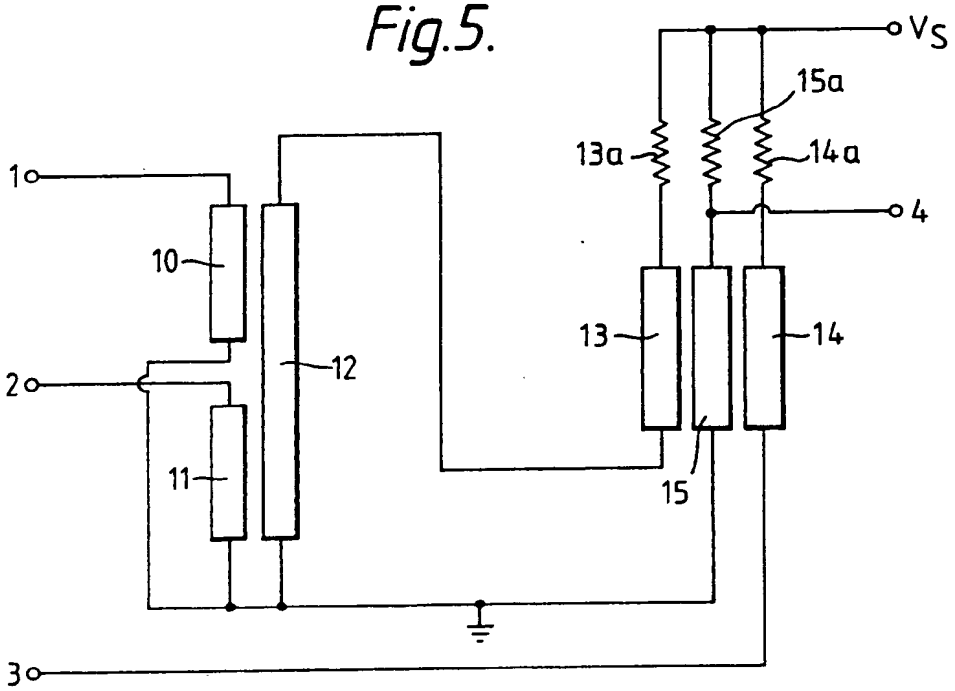
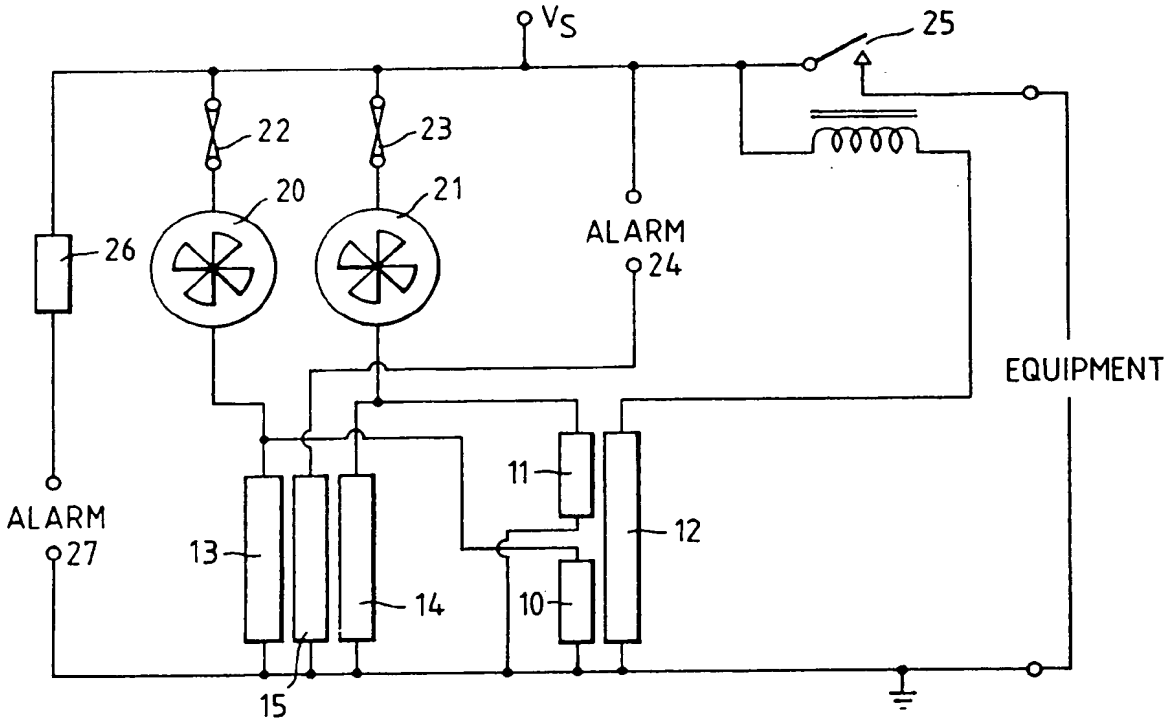


Fig.6.



SPECIFICATION

Thin film negative temperature coefficient resistor structure

This invention relates to electric circuit structures incorporating thin film negative temperature coefficient (NTC) resistors, known as NTC thermistors.

It has long been realised that the thermistor as a negative temperature coefficient resistor behaves to some extent like a gas discharge tube, and it is therefore a possible storage element, logic element, and oscillator.

This may be seen from the V/I characteristics of Fig. 1 which shows a voltage maximum in region II and a negative resistance region III. The region IV where the resistance becomes positive again is a region where the temperature of the thermistor is very high, and it is not usually considered as being in the normal operating range of the device.

The main respects in which this characteristic differs from that of a gas discharge tube are:–

(1) Speed of operation is very much lower.

(2) The provision of a triggering or third electrode has never been considered.

(3) There is no equivalent of the "burning" voltage of a gas tube; but on the other hand the ratio of Vmax to Vmin is probably greater than the ratio of the striking voltage to the burning voltage for a gas tube.

According to the present invention there is provided an electric circuit structure including at least a pair of thin film negative temperature coefficient (NTC) resistors electrically isolated one from the other but with mutual thermal coupling therebetween.

Such structures can form the basis of logic elements, with particular applications in circuit protection.

The production of thin film thermistors made by evaporating an intrinsic semiconductor onto a substrate gives a lead to a means of solving the frequency problem.

The time constant of a thermistor is given by

$$\tau = \frac{4.2hplbw}{K}$$

where h is the specific heat of the material in cal/g/°C
p is the density of the material in g/cc
l is the length in cm
b is the breadth in cm
w is the depth of a strip of semiconductor material (Fig. 2)
and K is the dissipation content in W/°C

Assuming heat losses are due to radiation and convection from only one surface of dimensions 1 and b (i.e. $w << 1, b$), we can write $K = k\,l\,b$ where k is a constant.

$$\therefore \tau = \frac{4.2\,hpw}{k}$$

For silicon and germanium $hp = 0.393$/cal/cc/°C and it will be assumed that:–
$k = 8$mW/°C/in² for a 20°C rise in temperature
1.24×10^{-3} watts/°C/cm²
$= 1.3\,w \times 10^{3}$ secs.

Fig. 3 includes a graph of τ against w from which it may be seen that w would have to be of the order of 0.1 micron to obtain a time constant of practical value, however, this is quite within the bounds of practicality. The resistance of a layer of intrinsic germanium (47 ohm cm at 300°K) is also shown in Fig. 3, for $1 = b = 1$ cm, as a function of w.

Apart from w the only other factor affecting τ over which the designer has any control is K. By evaporating the germanium on a very thin insulating base backed with copper, it is possible to increase the effective radiating surface, and hence increase K perhaps by an order of magnitude. However, the figure given for K above assumes that the surface is approaching that of a black body, whereas the surface is highly reflecting to light and its behaviour at infra-red is not known. It is also assumed that the laws of radiation apply equally to a sheet which is thin compared with the radiation wavelength. There is a need, therefore, to regard the figure of 8mW/°C/in² with caution, but to remember that to some extent is under the control of the designer.

The resistivity p_R is given by

$$PR = \frac{A}{T^n} \exp \frac{E}{2kT}$$

where E is the energy gap; 0.72 eV for Ge and 1.12 eV for Si in monocrystalline form
n is a number which depends on the behaviour of mobility with temperature (under some circumstances n can be very near zero).
A is a constant
and T is the absolute temperature

$$\frac{1}{PR}\frac{dpR}{dT} = \alpha = \frac{-n}{T}\frac{E}{2kT^2}$$

$= -4.8\%/°C$ for Ge at 300 K
$= -7.4\%/°C$ for Si at 300 K
assuming n = 0 or is very small.

It is important that the temperature coefficient should be as high as possible. One possible method of improving the temperature coefficient would be, after evaporating the film, to heat the germanium to melting point and let it cool under controlled conditions so that it becomes polycrystalline instead of amorphous.

The choice between silicon and germanium could be influenced by the temperature coefficients obtained in practice for an evaporated film, but it an adequate temperature coefficient can be obtained with germanium (e.g. $-3\%/°C$) it could be preferred in some applications because of its lower intrinsic resistivity. It will appear later the lower resistivity results in lower operating voltages.

An important parameter is the voltage maximum (region II in Fig. I) as this has a direct bearing on the voltages and power levels in any practical circuit.

It may be shown that:–

$$V_{max} = \sqrt{\frac{\rho_R L}{wb} k (T_1 - T_A) \exp \frac{B(T_A - T_1)}{2T_1 T_A}}$$

where T1 is the temperature of the thermistor when V = Vmax and is given by

$$T_1 = \frac{B}{2}\left(1 - \sqrt{1 - \frac{4T_A}{B}}\right)$$

where TA is the ambient temperature and $B = \alpha T_A^2$ where α is the temperature coefficient at $T = T_A$ (B is assumed independent of temperature and is related to the effective energy gap).

Fig. 4 shows $(T_1 - T_A)$ against α for $T_A = 300°$ K. It is clear from this graph that to keep $T_1 - T_A$ to a reasonable value, an alpha value of at least 3%/°C is desirable.

Given α and assuming K = 1bk,

$$vmax \frac{\alpha 1.}{\sqrt{W}}$$

Thus for a given film thickness Vmax is dependent only on the length of the strip.

Fig. 3 shows Vmax plotted for 1 = 1cm and $\alpha = 3\%/°C$ at TA = 300°K. The power dissipated when V = Vmax will be 1.25×44 mW cm^2 = 55 mW cm^2. In the "primed" condition (region I) a strip would be biased with a voltage slightly less than Vmax and could have an area considerably less than 1 cm^2 so the dissipation could probably be reduced to something of the order of 5mW. In the conducting region (region III) the dissipation will depend on the "on" resistance required and is limited by the temperature at which V = Vmin. The dissipation may be at least 5 times the "off" value.

The resistance ratio is of considerable importance and is given by:—

$$A = \exp\frac{B(T_2-T_0}{T2To}$$

where TO (<T1) is the temperature in region I and T2 (>T1) is the temperature in region III

For TO = 350°K, T2 = 450°K, B = 270°K, A = 9 times; doubling B or α would cause A to increase to over 70. So here again the importance of a large temperature coefficient of resistance is obvious.

A practical value for the upper limit of T2 is not known at present. As germanium melts at 958°C there seems to be no reason why operation at 400 or 500°C should be impossible. The resistance temperature characteristics has not been investigated above about 150°C. The observed temperature coefficient of 1.5%/°C appears to be independent of temperature up to 150°C. The above calculations are based on constant B rather than constant α, and are conditional on the assumption that a larger temperature coefficient can be obtained in practice, and that this temperature coefficient varies with temperature.

As has already been observed, NTC thermistors as logic elements, compared with silicon integrated circuits, are at a disadvantage because of a) low speed, and b) they have only two terminals. Other disadvantageous factors are c) their sensitivity to ambient temperature, and d) high operating voltage.

There are however, applications where a single logic function is required where the NTD thermistors could be useful and its advantages are then:

a) High noise immunity

b) Ability to work direct from an unrectified a.c. supply or a halfwave rectified unsmoothed supply.

However, logic using two terminal negative resistance devices usually demands a multiphase clock. To overcome this complication the present invention proposes the use of mutual thermal coupling between devices. This has the added advantages of enabling the input to be isolated from the output if so required.

Embodiments of the invention are now described with reference to Figs. 5–7 of the accompanying drawings in which:–

Fig. 5 illustrates general examples of logic structures utilising mutually coupled NTC thermistors.

Fig. 6 illustrates a fan failure detection arrangement using NTC thermistor logic structures, and

Fig. 7 illustrates geometrie of NTC thermistor logic structures.

Fig. 5 shows a combination of AND and OR logic gates constructed of NTC thermistors. The AND gate comprises two input thermistors 10, 11 each in mutual thermal coupling with an output thermistor 12. This works as follows. If a logic '1' is applied to both input terminals 1 and 2 simultaneously this causes sufficient heating of thermistor 12 for the latter to switch from its low current region (region I in Fig. 1) to its negative resistance region (III in Fig. 1) in relation to a fixed voltage applied across thermistor 12. A logic '1' applied to terminal 1 or terminal 2 alone will provide insufficient heating of thermistor 12 to cause breakdown. For the AND gate structure the mutual thermal coupling of each of the input thermistors 10 and 11 is with substantially one only of the two serially connected half sections of the output thermistor 12. For the OR gate structure thermistors 13, 14 are each in mutual thermal coupling with substantially one only of the two parallely connected half sections of the output thermistor 15. Thus a logic '1' applied to either thermistor 13 or thermistor 14 alone will provide sufficient heating of thermistor 15 to cause breakdown. Note that this arrangement will only function as and INCLUSIVE–OR gate. The two gates in Fig. 5 are illustrated in a combined AND/OR arrangement. A stable supply voltage V_s is applied to via impedances 13a, 14a and 15a such that all the thermistors are held in an initial state in region I just below the switching voltage II (Fig. 1). Subsequent application of a logic level '1' to either inputs 1 and 2 together or to input 3 results in breakdown of thermistor 15 to cause an output at terminal 4.

It is not possible to go on cascading such circuits without either an inverting device e.g. a transistor or the elaboration of multiphase clocking. Hence the need to concentrate on fairly simple logical operations where perhaps relays might otherwise be used.

It should be noted that in Fig. 5 is is necessary to interrupt the power supply in order to reset the logic. Working from a half wave rectified unsmoothed a.c. supply would be one way of achieving reset. On a 50Hz unrectified supply reset would occur as the voltage went through zero if the thermal time constant of the thermistor were much less than 10ms.

An example of a possible application is shown in Fig. 6. An equipment is coooled by two fans 20, 21. If either fan's fuse 22, 23 blows the equipment continues to function but an alarm 24 is given. If both fans fail the equipment is turned off automatically. The inputs to the AND and OR gates are low resistance elements in series with the fans which can be fabricated as one

continuous film for each fan. They would be thermally coupled with different geometries to the OR and AND elements. The OR element could, for example, extinguish a light if one fan failed and the AND element would cause a relay 25 to remove the voltage from the equipment being protected if both fans failed. A further element 26 might be mounted in the cooling air flow which could be used to detect excessive outlet air temperature and provide another alarm indication 27.

Fig. 7 shows the geometries of typical NTC thermistor logic structures.

Such devices could be fabricated either by deposition on opposite sides of a thin substrate or by deposition of an NTC device followed by an insulating layer (e.g. silicon oxide) followed by the deposition of another NTC device on top of the first.

This latter method is the one illustrated in Fig. 7. For the OR gate two input thermistors 30, 31 are deposited over an output thermistor separated into two halves 32, 33. The two half sections 32 and 33 are electrically in parallel and may be either separated as shown or are continuous element (not shown). Heating of either output thermistor alone by its superposed input thermistor results in a through circuit between the output terminals. In the AND gate structure the output thermistor 34 has two input thermistors 35 and 36 superposed, one over each half of thermistor 34. Heating of substantially the whole of thermistor 34 by both thermistors 35 and 36 simultaneously is required to switch thermistor 34. Deposition of thin film thermistor devices can be effected by sputtering techniques.

CLAIMS

1. An electric circuit structure including at least a pair of thin film negative temperature coefficient (NTC) resistors electrically isolated one from the other but with mutual thermal coupling therebetween.

2. An electric circuit structure according to claim 1 including a third thin film NTC resistor electrically isolated from and in mutual thermal coupling with one of the pair of NTC resistors, the arrangement being such that heating of one of the pair of NTC resistors and the third NTC resistor by voltages applied thereto results in each one of the electrically heated resistors heating by virtue of the mutual thermal coupling a different one half of the serially connected halves of the other NTC resistor of the pair.

3. An electric circuit structure according to claim 1, including a third thin film NTC resistor electrically isolated from and in mutual thermal coupling with one of the pair of NTC resistors, the arrangement being such that heating of one of the pair of the resistors or the third resistor alone by a voltage applied thereto results in each one of the electrically heated resistors heating by virtue of the material thermal coupling a different one half of the parallely connected halves of the other NTC resistor of the pair.

4. An electric circuit structure including two structures each as claimed in claim 1, with one resistor from each pair being connected together electrically in parallel.

5. An electric circuit structure according to any preceding claim including means for biassing the NTC resistors of the structure to a point just below the switching region of the resistors.

6. An electric circuit structure substantially as described with reference to Figs. 5–7 of the accompanying drawings.

7. A logic arrangement including mutually thermally coupled thin film negative temperature coefficient resistors.

8. An electrical equipment protection arrangement incorporating thin film negative temperature coefficient resistors with mutual thermal coupling therebetween substantially as described with reference to Fig. 6 of the accompanying drawings.

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